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10/672,186	09/26/2003	Michael Thomas Greene	51249/RAG/Z74	9829

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CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
MURRAY, DANIEL C	
ART UNIT	PAPER NUMBER
2443	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,186	GREENE, MICHAEL THOMAS	
	Examiner	Art Unit	
	DANIEL C. MURRAY	2443	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

Claim 1 recites no steps defining the method. It appears **claim 3** defined the steps of the method. The Examiner suggests including **claim 3** in its entirety in **claim 1** in order to recite a proper method.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-6 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. **Claims 2-6** are rejected by virtue of their dependency on **claim 1.**

Claims 1-6 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to particular machine, or (2) transform underlying subject matter (such as an article or material) to a different state or thing. See page 10 of In Re Bilski 88 USPQ2d 1385. The claims are neither positively tied to a particular machine that accomplishes the claimed method steps nor transform underlying subject matter, and therefore do not qualify as a

statutory process. The method of determining the routing of interconnected regions of a routing problem… is broad enough that the claim could be completely performed mentally, verbally or without a machine nor is any transformation apparent.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claims 1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Andreev et al. (US Patent Publication # US 2001/0018759 A1)** in view of **Rostoker et al. (US Patent # 5,742,510).**

a) Consider **claim 1,** Andreev et al. clearly show and disclose, a method of determining the routing (figure2, abstract, paragraph [0002], paragraph [0088], paragraph [0091], paragraph [0096]) of interconnected regions (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]) of a routing problem by considering all required connections in parallel independently (figure2, figure 3, abstract, paragraph [0033], paragraph [0034], paragraph [0088], paragraph [0091], paragraph [0096]) and only attempting to resolve crossing conflicts only (figure 2, abstract, paragraph [0088], paragraph [0092], paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0190], paragraph [0211], paragraph [0215], paragraph [0277]) when at least some contextual information about a region and the paths that cross in the region has been assembled (figure2, figure3, figure 8h, figure 9, abstract, paragraph [0089], paragraph [0102], paragraph [0124], paragraph [0143], paragraph [0187], paragraph [0210], paragraph [214]).

Rostoker et al. show and disclose microelectronic circuit fabrication, and more specifically to an integrated circuit physical design automation system utilizing optimization process decomposition and parallel processing, wherein considering all required connections in parallel independently (figure 6, abstract, column 21 lines 27-38).

Therefore, it would have been obvious to one of ordinary skill in the art that the time the invention was made to incorporate considering all required connections in parallel independently, as taught by, Rostoker et al. into the system of Andreev et al. for the purpose of optimized placement (Rostoker; abstract).

b) Consider **claim 2,** and **as applied to claim 1 above,** Andreev et al. as modified by Rostoker et al. clearly show and disclose, the method according to claim 1, wherein resolving of crossing conflicts is attempted only (figure 2, abstract, paragraph [0088], paragraph [0092], paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0190], paragraph [0211], paragraph [0215], paragraph [0277]) when all possible relevant contextual information has been assembled (figure2, figure3, figure 8h, figure 9, abstract, paragraph [0089], paragraph [0102], paragraph [0124], paragraph [0143], paragraph [0187], paragraph [0210], paragraph [214]).

c) Consider **claim 3,** and **as applied to claim 1 above,** Andreev et al. as modified by Rostoker et al. clearly show and disclose, the method according to claim 1, comprising the steps of:

(a) defining, for each set of regions to be connected (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]), routing which represents a suitable manner of connecting them (figure2, abstract, paragraph [0002], paragraph [0088], paragraph [0091], paragraph [0096], paragraph [0190]), respecting only those crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) which have been explicitly registered with the set currently being considered (figure2, abstract, paragraph [0088], paragraph [0089]paragraph [0190]);

(b) examining connections across shared boundaries (paragraph [0148]);

(c) collating all such proposed routing and resolving any crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) in a symmetric manner (figure 2, abstract, paragraph [0033], paragraph [0089], paragraph [0091], paragraph [0096]);

(d) registering such crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) with the sets of regions which will be required to respect them on the next pass (figure 2, abstract, paragraph [0033], paragraph [0088]);

(e) repeating steps (a) to (c) until a sufficient completion and quality of routing solution is attained (paragraph [0092]); and

(f) converting the routing into suitable geometric representations of routing paths in a way which takes all desired routing into account symmetrically and simultaneously (figure 2, figure 3, figure 9, figure 10, figure 11a, abstract, paragraph [0033], paragraph [0038], paragraph [0088], paragraph [0093], paragraph [0095], paragraph [0096]).

d) Consider **claim 4**, and **as applied to claim 3 above,** Andreev et al. as modified by Rostoker et al. clearly show and disclose, the method according to claim 3, in which the regions are polygons (figure 11a, figure 11b, figure 11c) and the shared boundaries are edges (figure 11a, figure 11b, figure 11c, figure 11d, paragraph [0148]).

e) Consider **claim 5,** and **as applied to claim 1 above,** Andreev et al. as modified by Rostoker et al. clearly show and disclose, the method according to claim 1, wherein the interconnected regions (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]) are regions of an electrical circuit (figure 1, paragraph [0015], paragraph [0033], paragraph [0034]).

f) Consider **claim 6,** Andreev et al. as modified by Rostoker et al. clearly show and disclose, a computer-implemented method (paragraph [0034], paragraph [0329]) of determining the routing (figure2, abstract, paragraph [0002], paragraph [0088], paragraph [0091], paragraph [0096]) of interconnected regions of a routing problem (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]), the interconnected regions (figure 11a, figure 11b, figure 11c, figure 11d, abstract,

paragraph [0148]) being regions of an electrical circuit (figure 1, paragraph [0015], paragraph [0033], paragraph [0034]), by considering all required connections in parallel independently (figure2, figure 3, abstract, paragraph [0033], paragraph [0034], paragraph [0088], paragraph [0091], paragraph [0096]) and attempting to resolve conflicts only (figure 2, abstract, paragraph [0088], paragraph [0092], paragraph [0145], paragraph [0190]) when at least some contextual information about a region and the paths which cross there has been assembled (figure2, figure3, abstract, paragraph [0089], paragraph [0102], paragraph [0124]).

Response to Arguments

7. Applicant's arguments filed 02APR2009 have been fully considered but they are not persuasive.

Applicant argues that "…in Rostoker, the placement and routing is for cells on a chip, not components on a printed circuit board (PCB) as in the present application. In addition, the described routing is channel routing, not gridless PCB routing."

In response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the features upon which Applicant relies (i.e., components on a circuit board, gridless PCB routing) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant's argument that in Rostoker, the placement and routing is for cells on a chip, not components on a printed circuit board (PCB) as in the present application, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in

order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Rostoker clearly discloses routing connections in connection with integrated circuit design (Rostoker; column 1 lines 14-18, column 14 lines 13-27, column 16 lines 27-40) therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker and Andreev since both concern integrated circuit design and as such, both are with in the same environment (Andreev; paragraph [0002], Rostoker; column 1 lines 14-18), more particularly both clearly teach the routing of paths in integrated circuits (Andreev; abstract, paragraph [0015] Rostoker; column 14 lines 13-27, column 16 lines 27-40). Furthermore, while it is possible that Rostoker is mainly directed towards routing cells on a chip it is clear from Rostoker that the methods are applicable to problems even outside the scope of integrated circuit design (column 13 lines 47-67, column 14 lines 1-4).

Applicant argues that the combination of Andreev and Rostoker do not teach "…all nets can be routed fully in parallel, independently and simultaneously." and "…that the method of Applicant's claims 1-6 would not be obvious to a worker skilled in the art who considered the Andreev and Rostoker references. The proposed combination would not be obvious and, even if attempted, would not yield the claim method."

In response to Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Andreev clearly discloses the routing of nets in an integrated circuit design (abstract, paragraph [0015], [0088], [0091], [0096]), the routing is done in parallel, independently, and substantially simultaneously.

Rostoker clearly discloses microelectronic circuit fabrication, and more specifically an integrated circuit physical design automation system utilizing optimization process decomposition and parallel processing, wherein considering all required connections in parallel, independently, and simultaneously (figure 6, abstract, column 13 lines 47-50, column 14 lines 13-27, column 21 lines 27-38).

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker and Andreev since both concern integrated circuit design and as such, both are with in the same environment (Andreev; paragraph [0002], Rostoker; column 1 lines 14-18), more particularly both clearly teach the routing of paths in integrated circuits (Andreev; abstract, paragraph [0015] Rostoker; column 14 lines 13-27, column 16 lines 27-40).

Therefore, it would have been obvious to one of ordinary skill in the art that the time the invention was made to incorporate independent, parallel, and simultaneous routing, as taught by, Rostoker into the system of Andreev for the purpose of routing of interconnected regions on a PCB, thereby allowing all connections to be considered simultaneously.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker and Andreev since both concern integrated circuit design and as such, both are with in the same environment (Andreev; paragraph [0002], Rostoker; column 1 lines 14-18),

more particularly both clearly teach the routing of paths in integrated circuits (Andreev; abstract, paragraph [0015] Rostoker; column 14 lines 13-27, column 16 lines 27-40).

Furthermore, the Examiner fails to see how it would not be obvious to combine Rostoker and Andreev when by Applicant's own admission "the Rostoker parallelisation would indeed be a sensible way to implement a parallelisation framework to support the separate routing tasks described in Andreev…" while Applicant goes on to argue that "...this would still not make Andreev able to route the nets fully in parallel, independently and simultaneously." the Examiner respectfully disagrees; Andreev clearly discloses the routing of interconnected regions independently, in parallel, and substantially simultaneously and Rostoker clearly discloses routing in parallel and simultaneously and since both Andreev and Rostoker concern integrated circuit design and as such, both are with in the same environment, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate independent, parallel, and simultaneous routing, as taught by, Rostoker into the system of Andreev for the purpose of allowing all connections to be considered simultaneously.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- 5,875,117
- US 6,877,146 B1
- US 6,928,633 B1
- US 6,557,145 B2

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL C. MURRAY whose telephone number is 571-270-1773. The examiner can normally be reached on Monday - Friday 0800-1700 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tonia Dollinger can be reached on (571)-272-4170. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DCM/
Examiner, Art Unit 2443

/Tonia LM Dollinger/

Supervisory Patent Examiner, Art Unit 2443